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Mitigating Wire Short Defect on LGA Device through Substrate Design Optimization

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Authors' contributions

This work was carried out in collaboration amongst the authors. All authors read, reviewed and approved the final manuscript.

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ABSTRACT

During new product development of a substrate land grid array (LGA) device, issues were encountered at wirebonding process due to design constraints. This paper is focused on addressing the wire-to-wire short defect during wirebonding process of the first bond. Wirebond process optimization was comprehensively employed, but eventually recommended to have a substrate redesign with relocated bond fingers to increase the wire angle (less steep) between the first bond and the second bond. With the improvement done in the substrate design and through wirebond process optimization, wire-to-wire short defect occurrence was successfully eliminated.

Keywords: Bond finger; LGA; substrate; wire short; wirebond process.

1. INTRODUCTION

Semiconductor devices on LGA packaging platform are continuously developed and improved to deliver high quality and robust products for various applications. A common direction of semiconductor manufacturing companies is to increase the production yields and maintain high quality while minimizing the wastage and assembly rejections. Wirebonding process is one of the challenging processes in semiconductor industry for

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integrated circuit (IC) assembly [1-5], responsible for attaching the wires to provide electrical connections through combination of heat, pressure and thermosonic energy. With the new wirebonding layout with 40 degrees angle of wire located at the upper right of the unit, a big challenge exists to run the lot or to process this type of technology especially in wirebonding process. The paper presents a solution to successfully process this type of technology in IC assembly manufacturing by relocating the bond finger of the carrier or substrate. To guarantee its integrity during production run wirebond process is incorporated with a multiple of criteria such as ball size, ball height, ball aspect ratio, wire pull test, ball shear test, stitch pull test, loop height, intermetallic coverage, and contact angle. The wirebond criteria is performed after machine conversion or setup to ensure that the product is reliable when subjected to reliability tests. Fig. 1 shows the actual representation of reject unit.

A typical assembly process flow for the LGA device is given in Fig. 2 with processes starting from pre-assembly to singulation. Highlighted is the process affected with the encountered issue.

Wire-to-wire short occurrence is the top major assembly reject during the attachments of wire especially on the first bond process and this was seen during the lot processing phase of the package at wirebonding process station. The wire-to-wire shorting issue is cause by a tight degree angle of wires during the attaching of wires on the first bond. Several factors may contribute to the wire-to-wire shorting effect such as the loop height is inconsistent and die placement is out of tolerance. Visual inspection of the actual unit using the old design of substrate has done 100% visual inspection to identify the reject. The device in focus used a Gold (Au) wire. During the development stage of the device in wirebonding process, relocation of bond finger of the substrate was employed and comprehensively characterized to address the issue of wire-to-wire shorting occurrence. In the end, the major challenge and motivation is to process the qualification lot with speed without compromising the quality of our customers.

2. METHODS AND RESULTS

With the extensive process characterization and design optimization for the LGA package, the issue of wire-to-wire shorting in wirebond process was eventually mitigated. The process optimization is comparable to other works done in [6-8], but this time the significant contribtuion is through the substrate design-level improvement. The improved and enhaced process solution was formulated by relocating the bond finger of the substrate to increase the wire angle (less steep) during the attachments of wires. Fig. 3 shows the actual photo of wire formation using the enhanced substrate design.

Ulitmately, with the improvement done on the substrate design and with the process optimization, no wire-to-wire shorting occurrence was observed during wirebonding process. A 100% visual inspection during the ejection of the substrate is not anymore needed, thus saving resources and time. Moreover, faster delivery of units and business movement could be realized.

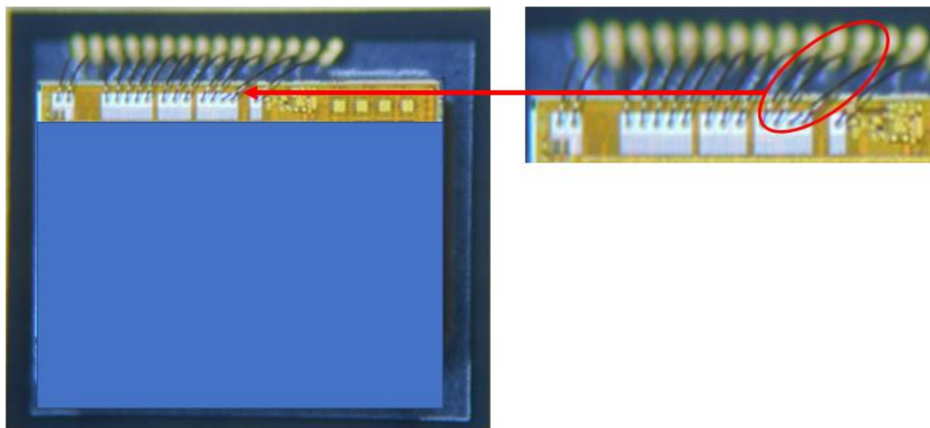

Fig. 1. Actual reject unit with wire-to-wire shorting

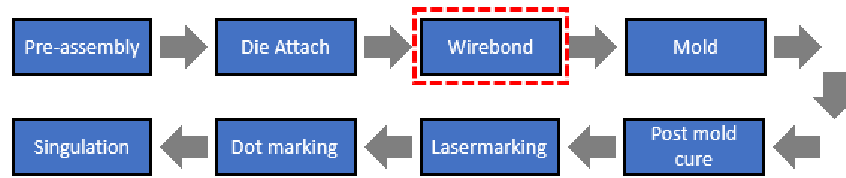

Fig. 2. Assembly process flow

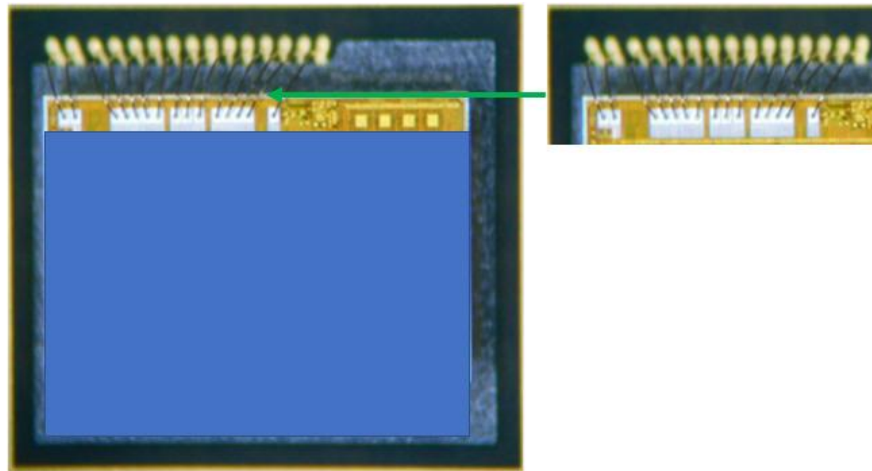

Fig. 3. Actual photo of wire formation with no wire-to-wire shorting, using the enhanced substrate design

3. CONCLUSION

Substrate design improvement and wirebonding process optimization were employed to address the wire-to-wire shorting defect occurrence during the process. By relocating the critical bond fingers of the substrate, a stable first bond during wirebonding process was successfully established. The solution through design-and-process improvement could be adapted on other semiconductor devices with comparable configuration. Comparison of existing works and improvement should also be included for added analysis. Discussions and learnings shared in [9-12] are useful in reinforcing robustness and optimization of package design and assembly processes particularly at wirebonding process.

DISCLAIMER

The products used for this research are commonly and predominantly used products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Tan CE, et al. Challenges of ultimate ultra-fine pitch process with gold wire & copper wire in QFN packages. 36th International Electronics Manufacturing Technology Conference. Malaysia. 2014;1-5.
2. Lall P, et al. Reliability of copper, gold, silver, and PCC wirebonds subjected to harsh environment. IEEE 68th Electronic Components and Technology Conference (ECTC). USA. 2018;724-734.
3. Hong SJ, et al. The behavior of FAB (free air ball) and HAZ (heat affected zone) in fine gold wire. Advances in Electronic Materials and Packaging (Cat. No.01EX506). South Korea. 2001;52-55.
4. Descartin M, et al. Non-continuous IMC in copper wirebonding: Key factor affecting the reliability. 6th International Conference

on Electronic Packaging Technology (ICEPT). China. 2015;403-407.
5. Sameoto D, et al. Wirebonding characterization and optimization on thick film su-8 mems structures and actuators. Transducers 2007-2007 International Solid-State Sensors, Actuators and Microsystems Conference. France. 2007; 2055-2058.
6. Moreno A, et al. Wire shorting elimination through wirebond process optimization of semiconductor sensor device. Journal of Engineering Research and Reports. 2020; 13(4);10-14.
7. Pulido J, et al. Wirebond process improvement with enhanced stand-off bias wire clamp and top plate. Journal of Engineering Research and Reports. 2020;9(3):1-4.
8. Moreno A, et al. Enhanced loop height optimization for complex configuration on QFN device. IEEE 22nd Electronics Packaging Technology Conference (EPTC). Singapore. 2020;182-184.
9. Sumagpang Jr. A, et al. Non-stick on pad defect reduction through clamp and insert design augmentation. Journal of Engineering Research and Reports. 2020; 12(2):37-45.
10. Tran TA, et al. Fine pitch probing and wirebonding and reliability of aluminum capped copper bond pads. IEEE 50th Electronic Components and Technology Conference (ECTC). USA. 2000;1674-1680.
11. Angeles A, Arellano IH. Understanding non-stick on lead wirebond failure due to leadfinger surface roughness. International Research Journal of Advanced Engineering and Science. 2019;4(2):49-54.
12. Gomez FR, et al. Augmented leadframe design for stable multi-wire ground bonding. Journal of Engineering Research and Reports. 2021;20(3):1-5.

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